

## INTRODUCTION

It is a well-known problem in low-temperature resistance thermometry, that resistive low-temperature sensors are very sensitive to unwanted heating by high frequency interference, if such interference somehow manages to reach the cooled resistor via its measurement leads. Heating raises the temperature of the sensor above its surroundings resulting in erroneous readings, which give the impression that the cryostat does not reach its expected temperature. If good shielding and making the sensor wires as short as possible do not solve the heating problem, there is only one method left: to filter the measurement lines.

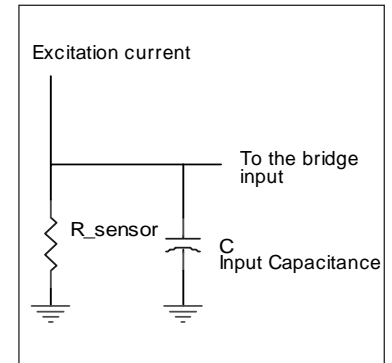
Modern dilution cryostats may have base temperatures lower than 50 mK. All resistive sensors, that are useful at and below this level, have a middle to high resistance. This means that the filter capacitance must be low so that C does not affect the AC measurement. If the RF filter is of the "RC" type, the resistance should then be high enough for effective filtering at the low end of the RF range. Unfortunately, the filter resistors are at room temperature. If higher than few kilo-ohms, they generate thermal noise that will exceed all other noise sources. One may then want to use an "LC" type filter, and use inductors instead of resistors. The danger is, however, that the inductor becomes a part of a resonant circuit, and great care is needed to ensure that the Q-value of the input remains low and that there is no significant interference at the tuning frequency.

It would be best if one could use resistors below 1 kilo-ohm in the filters and just select sufficiently large capacitors.

This article deals with the ways how an ideal capacitance affects an AC resistance measurement, when it is based on either sine wave or square wave. It may also help in understanding the differences between various types of cryogenic resistance bridges on the market.

## The parallel connection of R and C

Let us assume that the measuring instrument has generated a sinusoidal excitation current  $I_E$  which is fed to the sensor in the cryostat. If the capacitance is zero or negligible, the voltage drop across



$R_S$  is simply  $V_O = I_E * R_S$ , and as a low-frequency sine wave, it is quite easily measurable. In reality,  $V_O$  is extremely low, and a lot of amplification is required before it can be quantified. The present discussion concentrates only to the capacitive effects, so that we can forget most of the actually required measuring techniques.

If the input capacitance is not negligible, we have to replace  $R_S$  by the parallel connection of  $R_S$  and C. For a sinusoidal excitation current of angular frequency  $\omega$ , the output voltage is

$$(1) \quad V_O = I_E * Z = I_E * \frac{R_S * (1 / j\omega C)}{R_S + (1 / j\omega C)}$$

where j is the imaginary unit. With little calculation,  $V_O$  can be divided in real and imaginary parts:

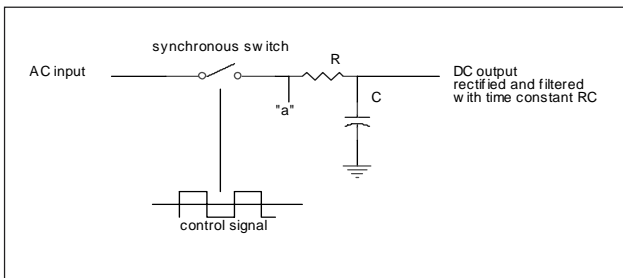
$$(2) \quad V_O = \frac{I_E \cdot R_S}{(1 + (\omega C R_S)^2)} - j * \frac{I_E \cdot \omega C R_S^2}{(1 + (\omega C R_S)^2)}$$

In addition to  $R_S$ , the above equation has also a second unknown, C. It is unknown, because we do not know its magnitude exactly. Capacitors have often a 10% tolerance and they are quite sensitive to temperature changes.

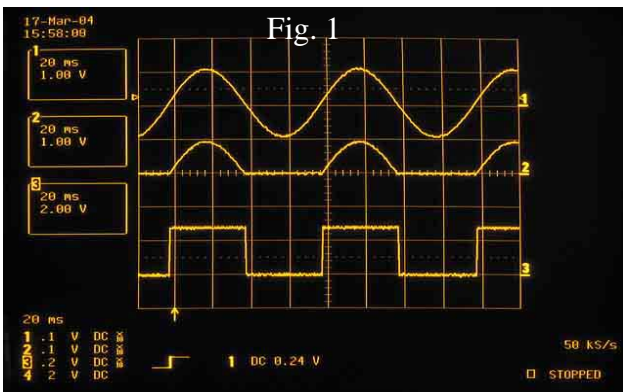
We need two equations for solving two unknowns, and the technique required now is called "synchronous detection" or "phase-sensitive detection". This method is familiar to those who have worked with lock-in amplifiers. It is also used in all AC resistance bridges.

**Phase-Sensitive Detection**

The picture below shows the simplified idea of a phase-sensitive detector (PSD). The digitally controlled switch closes whenever the control signal is high. When the switch is closed, the AC input signal is accumulated in the filter at a speed that depends on the filter's RC time constant.



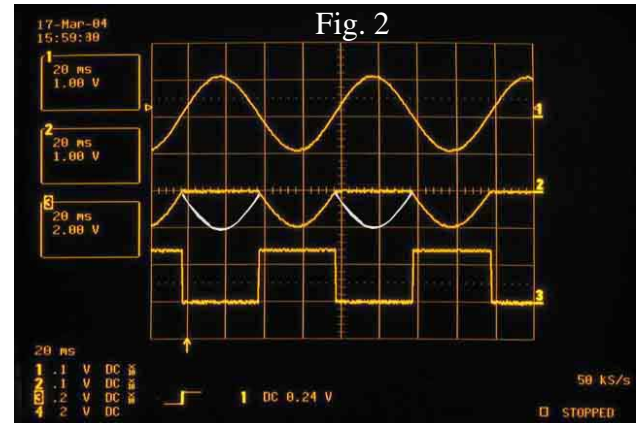
The following oscilloscope screenshots show, how the system works. The oscilloscope probe was connected to point "a" and the output was temporarily connected to ground so that the rectified waveform has its correct shape.



The upmost trace is the AC input signal, symmetrical around zero. The lowest trace is the digital control signal. Its high state enables the analog switch, letting the signal to proceed to the output. This picture was taken when there is no phase shift between the control and input signals. In other words, detection was made at 0 degree angle.

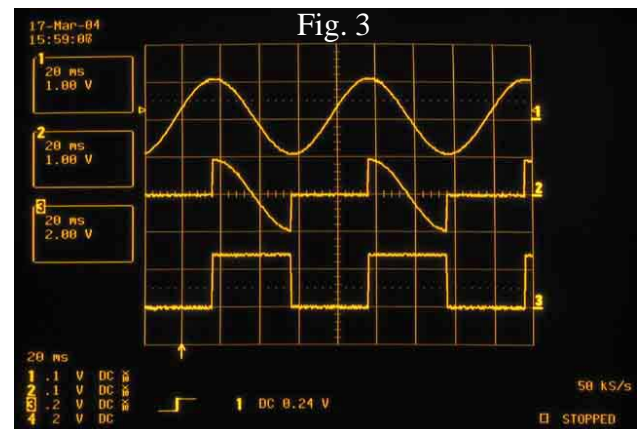
For simplicity, the above traces show the half-wave rectification, where only one half of the input signal is used. It is evident from the picture, that a

long filter time constant is required to get a smooth average. This is why full-wave rectification is generally preferred. Then one needs to invert the input signal and to use a switch that can select either the normal or the inverted signal in turn.



This screenshot is the same as before, except that now the phase angle is 180 degrees, and the switch picks only the negative half cycles. The white curve pieces show, how the output would look like in case of full-wave rectification.

The filter stores an average of the output signal. In the first case, it was a positive voltage, in the second case, it was negative.



If the phase angle is 90 degrees, the resulting average is zero (the above screenshot).

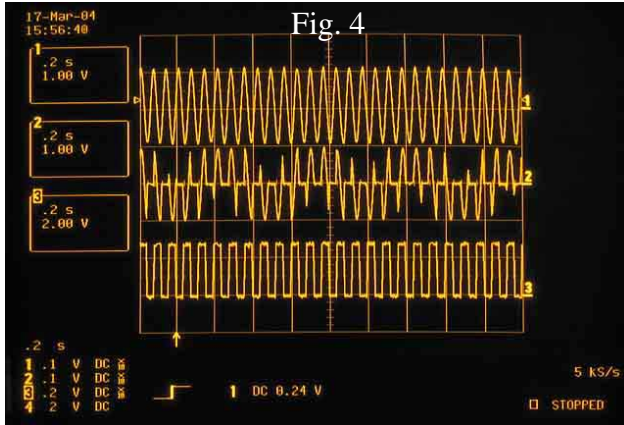


Fig. 4

In the above examples, both the input signal and the control signal had the same frequency, 12.5 Hz, and only the relative phase angle was changed.

If the input and control signals have different frequencies, the output changes its shape continuously. The middle trace of the above picture shows, what happened when the input frequency was shifted from 12.5 to 14.5 Hz. If the output is filtered with a time constant that is not very long, we get a sinusoidal signal whose frequency is  $14.5 - 12.5 = 2$  Hz. Making the time constant long enough, the amplitude of the **output beat** can be made arbitrarily low.

The two important conclusions for phase-sensitive detection are:

- If the input and control signals have different frequencies, the beating signal can be attenuated by filtering.
- If the two signals have exactly the same frequency (they originate from the same source), the rectification result depends on their relative phase shift. 0 and 180 degrees result in maximum and minimum, whereas 90 and -90 degrees result in zero.

### Using two PSDs

Electronic quantities, like voltages, are often expressed as complex numbers. The real part is related to a dissipative (resistive) component where the current through it and the voltage across it are in the same phase. The imaginary part is related to induc-

tive or capacitive (reactive) components, where the current and voltage are in 90 degrees phase shift.

In case of a capacitance, its voltage **lags** the sinusoidal charging current by 90 degrees. In case of an inductance, its voltage **leads** the current by 90 degrees.

Let us now recall equation (2). Suppose that we have access to the excitation current source so that we can get two control signals from there: one that is in exact phase with the current and one that comes 90 degrees later. We can then build a circuit that consist of two PSDs that rectify  $V_O$  in both the zero phase and in the -90 degrees phase (the latter is called "quadrature detection").

The two detection results are the real and imaginary components of the complex  $V_O$ :

$$(3) \quad \text{Re} = \frac{I_E \cdot R_S}{(1 + A^2)}$$

$$(4) \quad \text{Im} = \frac{I_E \cdot A R_S}{(1 + A^2)}$$

$$(5) \quad A = \omega \cdot C \cdot R_S$$

From (3) and (4) we get  $A = \text{Im}/\text{Re}$  and calculate it from the two detector voltages. Equation (3) gives then  $R_S = \text{Re} (1 + A^2)/I_E$ . Now that we know  $R_S$ , we can calculate C from (5):

$$(6) \quad C = \frac{A}{\omega R_S}$$

In a cryogenic resistance bridge, synchronous detection in the 0 degree phase is mainly needed for recovering the bridge unbalance signal from noise. If the capacitance is low, or if capacitive effects are not considered important, one may want to keep the instrument simple and to omit the quadrature detection. The detection result is then simply the real part of  $V_O$ , which depends on capacitance as

$$(7) \quad \text{Re} = \frac{I_E \cdot R_S}{(1 + \omega^2 \cdot C^2 \cdot R_S^2)}$$

A 1 nF capacitor would make a 1 MΩ resistor seem like 0.99 MΩ at 15.9 Hz frequency. The error is 1%, which is a lot for a precision instrument.

10 nF capacitance at 15.9 Hz drops the apparent resistance down to 500 kΩ.

Although the two-PSD method seems ideal on paper, it may not be that in practice.

If the capacitance is large, the detection results become small and accuracy suffers. For example, a 47 nF capacitor across a 1 MΩ resistor yields a real component that is only 1/23 of its zero-capacitance value. Because  $A=Im/Re$ , any possible offset terms or digitizing errors in measuring  $Re$  become significant when  $Re$  is small.

Moreover, the signal phase lags now by more than 75 degrees, and the output from the 0-degree PSD looks like that in the screen shot from 90 degree (Fig.3). The small  $Re$  value comes from the difference between almost equal positive and negative parts of the curve. It is evident that such a difference is very sensitive to any possible phase shift in the signal path.

The signal amplifier - which is always required when measuring a cryogenic sensor - should not contain any phase-shifting constructions, like filters or blocking of DC voltages by means of capacitors and bleed resistors.

### Measurement using square wave

The square waveform contains a spectrum of higher harmonic frequencies, and therefore it is commonplace to say, that it should not be used for this kind of measurements, where a significant capacitance loads the unknown resistance. This is true, but only partly.

Suppose that the excitation current in the figure on page 1 is changed from sine to square. Let the resistance be 1 MΩ and capacitance 1 nF. The output waveform appears somewhat rounded, and synchronous detection in 0° phase gives a value that is about 3.5% less than its zero-capacitance value. This is absolutely too much for a cryogenic resistance bridge, whose accuracy should be in the range 0.01% - 0.1%.

The shunted voltage  $V$  approaches the zero-capacitance voltage  $V_0$  exponentially with the RC time constant

$$(8) \quad V = V_0 \cdot (1 - e^{-t/RC})$$

When time  $t$  has reached the length of  $RC$ ,  $V$  has increased to 63% of its final magnitude and so on. Let the excitation frequency be now 12.5Hz, so that the length of a full cycle is 80 ms. Full-wave synchronous detection means that one of the two selection switches is open during each half cycle.

We can now reduce the capacitance effect by delaying the closing of each switch in turn for the time of 1/4 of the full cycle length, starting from each transition in the excitation current. In this example, the  $RC$  time constant was 1 ms, and the non-conducting time after the waveform edges is 20 ms. Because of the new delay, the time that is allowed for  $V$  to approach  $V_0$  is 20 time constants before the PSD is enabled, and from eq. (8) we can calculate that  $V$  is already correct to 0.999999998 when the switch closes. If the input time constant is doubled to 2 ms, the error would be  $5E-5$ . Note, that each synchronous switch conducts for 20 ms, which is equal to the 50 Hz mains cycle. Each cycle of a possible mains interference is therefore averaged to zero. In a 60 Hz country, the excitation is 15 Hz and switch times are correspondingly shorter.

This is essentially the technique that has been utilized in the AVS-46 and AVS-47 resistance bridges from Picowatt. The practical results are unfortunately not as good as predicted here, although they are much better than when using sine wave excitation but no quadrature detection. Two candidates for the less-than-predicted performance are the non-ideality of the capacitors and the always present small nonlinearity of electronics.

If the time constant is increased to 10 ms (1 MΩ || 10 nF), only two time constants are allowed for the transients to decay off, and the 14% error at the beginning of detection makes the measurement useless.

**Active Capacitance Compensation**

If one does not know the phase of a sine wave precisely, it is impossible to say or measure, whether its magnitude has been attenuated by capacitive shunting or not, because its shape remains the same. Surprisingly, the high-frequency contents of a square wave make possible a method for compensating most of the capacitive shunting. This method is based on the fact that capacitance changes the shape of the waveform instead of its phase.

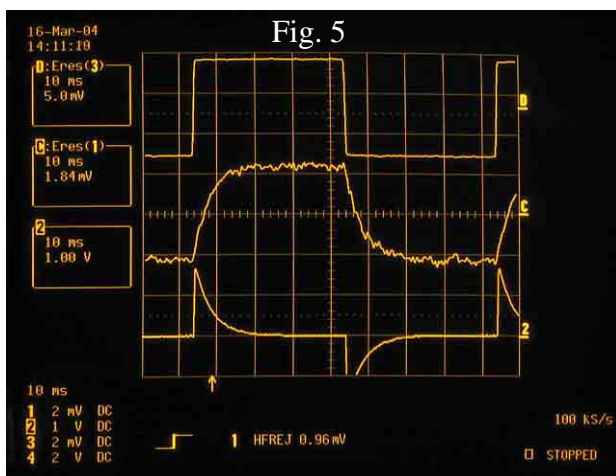


Fig. 5

The above screenshot shows waveforms of the excitation current (D) and the resulting voltage drop across the sensor of an AVS-47A resistance bridge (C). The excitation is an almost ideal square, whereas the 10 nF capacitance has rounded the voltage drop across 1 MΩ significantly. The rounded waveform looks noisy, because the digital oscilloscope had to use a large amplification to show the tiny voltage. The lowest trace (2) is what results when the two above voltages are compared by a differential preamplifier.

The idea of the automatic compensation circuit is to detect the peaks and to use the detection result for generating short pulses that quickly charge the input capacitance to such a voltage, that the rounded waveform becomes square again. When the sensor voltage drop is later detected after the 1/4 cycle delay time, it will have the correct value to a high accuracy.

The following discussion refers to the detailed schematic of the compensation circuit.

The comparison result, trace "2" in Fig 5, which is actually the AC OUT - output from the AVS-47A, is taken as input "A" to the compensation circuit. Any possible DC level in this output is blocked by capacitor C3. No separate bleed resistor after C3 is necessary, because R8, the input for the inverting stage U1D, serves as the bleed resistor.

The comparison spikes are buffered and fed to input 12 of the analog switch U3. The spikes are also inverted by U1D and fed to input 15 of U3. The next task is to take only the relevant parts of the positive spikes and send them to the integrator stage U1C, and to take the relevant parts of the inverted negative spikes and send also them to the integrator. In order to do so, we need control signals that are synchronous to the excitation current.

Signals **f** and **2\*f** are readily obtained from the synchronization logic of the AVS-47A and they are used for controlling the analog switch. The interesting states of control inputs A and B (C is grounded) at pins 11 and 10 of U3, are

- |   |   |   |
|---|---|---|
| B | A |   |
| 0 | 0 | all switches are open                   |
| 0 | 1 | all switches are open                   |
| 1 | 0 | inverted spikes are connected by X2     |
| 1 | 1 | non-inverted spikes are connected by X3 |

By feeding signal **f** to control input A, we take care that spikes resulting from excitation current transitions upwards are handled inverted and transitions downwards are handled non-inverted.

Signal **2\*f** cannot be used as such to control input B, because then we would integrate for 1/4 of cycle length after each transition; we want to integrate just the relevant parts of the spikes. This makes the circuit more capable of seeing only the spikes, and that is what we want. Because the integration time needs not be adjusted to any exact length, a simple derivation circuit of C5 and R12 is sufficient. There are two factors when selecting these components: 1) R12 must not load the CMOS signal too heavily, therefore its value cannot be less than about 10 kΩ and 2) C5 is chosen after R12 to give a suitable output pulse width.

**AC Resistance Measurement in Presence of Input Capacitance**

Derivation must not produce negative spikes, because they are not accepted by the CMOS control inputs. D2 is biased to about +0.7 V and D1 clamps signal "D" so that it cannot go too much in the negative direction.

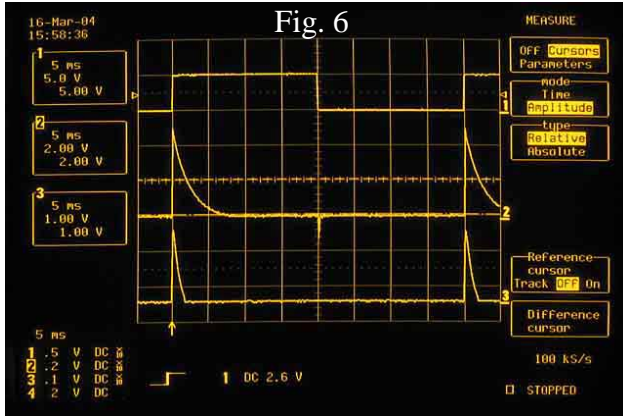


Fig. 6. above shows the control signal "E" ( $2 \cdot f$ ), control pulses "D" obtained by derivation, and the output "F" (lowest trace) from the analog switch in a case where the circuit has not yet managed to cancel the spikes. The threshold level of the CMOS control inputs is about 2.5V when the operating voltage is +5V. As shown by the output trace "3", the switches conduct for about 2 milliseconds after each transition. All output spikes are positive, because the down-going spikes have been inverted by U1D.

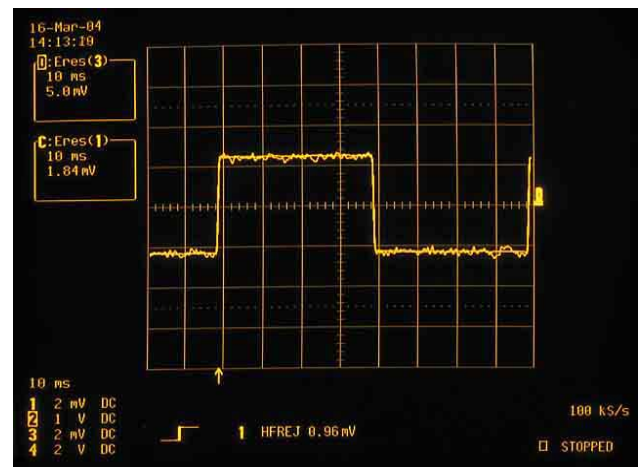
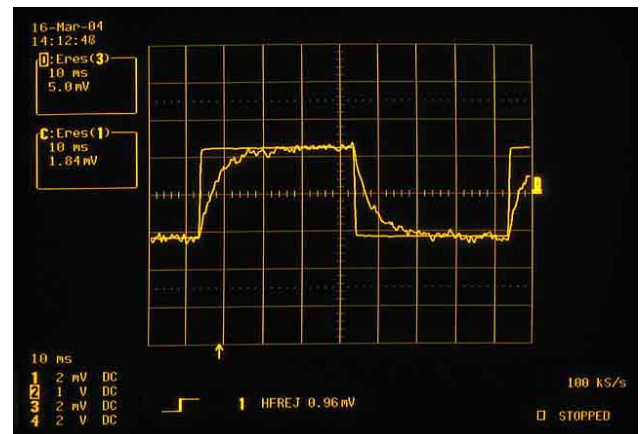
As long as signal "F" contains up-going comparison spikes, the integrator U1C slews downwards. Its output is a negative DC voltage. It is inverted by U1B and these two voltages are fed to inputs X0 and X1 of the second analog switch U2.

Signal "E" is applied to the control input A (pin 11) of U2. It selects either the inverted or non-inverted integrator voltage, and the resulting square wave, synchronous and in phase with the excitation current, is applied to C2. This is a rather small polystyrene capacitor, which passes only the rising and falling edges of output "J" to the chain of reference and sensor resistors of the resistance bridge.

Whenever conditions at the input of the AVS-47A change so that the voltage drop and the ideal-square feedback no longer have identical shapes, spikes appear and this circuit starts to change its integrator voltage either up or down until the spikes disappear again.

The present circuit is not ideal, as an analog circuit can never be. The main reason is perhaps, that the edges produced by the AVS-47A and edges produced by the compensation circuit are not exactly concurrent. Especially when the sensor resistance is low, it seems to happen, that the spikes do not disappear completely but are replaced by two very fast succeeding opposite spikes, whose average during the 2 ms integration time is zero. Although this looks bad, the effect is not dangerous, because the input time constant is short when the sensor resistance is low, and the peaks have good time to decay off.

Pictures 7 and 8 show the AVS-47A input of  $1 \text{ M}\Omega$  in parallel with a  $10 \text{ nF}$  capacitor, when the compensation circuit was disabled and when it was enabled.



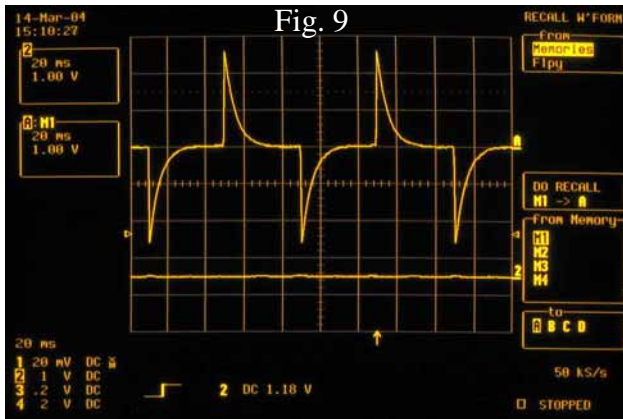


Fig. 9. above shows, how the signal at "AC OUT" changes when a 10 nF capacitance and a 1 MΩ resistance are in parallel, and the AVS-47A compensation circuit is disabled or enabled.

**Capacitors are different**

Results in compensating the input capacitance differ between various types of capacitors, and probably even between different lots of the same capacitor type and brand. The dissipative components in the capacitors are not usually exactly specified, typically only the maximum dissipation at one frequency is given. We tried some capacitors of different types:

resistance	1 MΩ	2 MΩ
type	error % of F.S.	
47 nF polystyrene	-0.025	-0.125
47 nF polyester	-0.2	-0.9
47 nF ceramic	-1.3	-5.25
1 nF ceramic	-0.025	-0.1

So be careful when designing an RF filter. Test the capacitors with the AVS-47A on the table before using them in your design. Polystyrene, and probably also polypropylene, capacitors may be the best for maintaining good linearity, but unfortunately they are not useful at high frequencies. Try a combination of a large PS or PP capacitor in parallel with a small ceramic or mica capacitor. Such a combination might give the best tradeoff between good frequency response and low resistive losses.

**Summary**

Both the sine and square waveforms can be used for accurate AC resistance measurements, even if the resistance is shunted by a parallel capacitance of unknown size.

In case of sinusoidal excitation current, the resulting voltage drop must be detected in both zero and quadrature phases. Calculation of the resistance from the detection results requires digital intelligence that is capable of performing floating point arithmetics. If the capacitance is high, the zero-phase detection result becomes small and sensitive to possible phase shift in the signal path. These facts can affect the accuracy of the measurement.

In case of square wave excitation, equally good - or even better - results can be obtained by using shape-based automatic compensation of the comparison spikes and delayed phase-sensitive detection. No calculations are required.

Regardless of the excitation waveform, resistive losses and non-ideality of capacitors limit the attainable accuracy. These effects depend very much on the capacitor's size and on its type.

